μA711C
DUAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

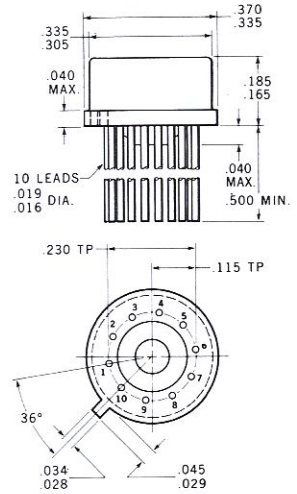
GENERAL DESCRIPTION - The μA711C is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The μA711C, which is similar to the μA710C differential comparator, is constructed on a 40-mil square silicon chip using the Fairchild Planar epitaxial process.

For full temperature range operation (-55°C to +125°C) see μA711 data sheet.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage		+14.0 V
Negative Supply Voltage		-7.0 V
Peak Output Current		50 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Strobe Voltage		0 to +6.0 V
Internal Power Dissipation	(Note 1)	300 mW
Operating Temperature Range		0°C to +70°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

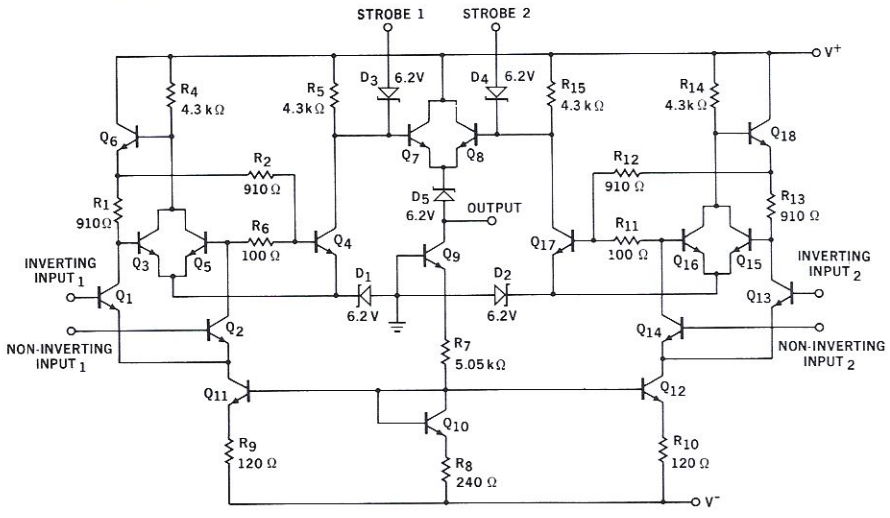
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-100) outline



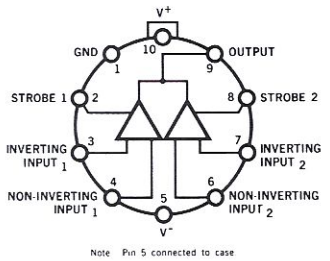
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F771139X

SCHEMATIC DIAGRAM



TO-100 CONNECTION DIAGRAM (TOP VIEW)



Note Pin 5 connected to case

Notes on page 2

* Planar is a patented Fairchild process.

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FAIRCHILD SEMICONDUCTOR
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ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0 V, V^- = -6.0 V unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max	Units
Input Offset Voltage	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$, V_{CM} = 0		1.0	5.0	mV
	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$		1.0	7.5	mV
Input Offset Current	V_{out} = +1.4 V		0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = -7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{strobe} = 100 mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	230	mW
The following specifications apply for 0°C $\leq T_A \leq$ +70°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$, V_{CM} = 0			6.0	mV
	$R_S \leq 200\,\Omega$			10	mV
Input Offset Current (Note 3)				25	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:

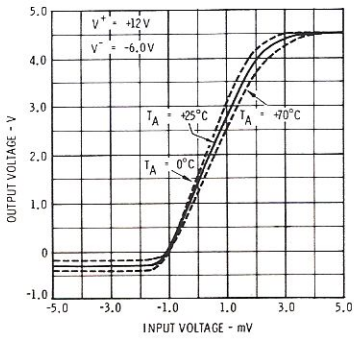
(1) Rating applies for ambient temperatures to +70°C.

(2) The response time specified is for a 100-mV input step with 5-mV overdrive.

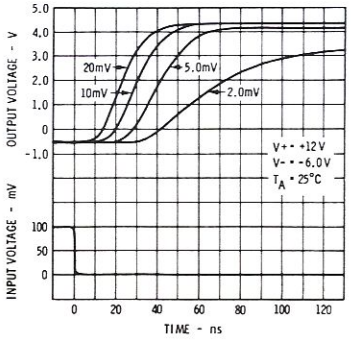
(3) The input offset voltage is specified for a logic threshold voltage of 1.5 V at 0°C, 1.4 V at +25°C and 1.2 V at +70°C.

TYPICAL ELECTRICAL CHARACTERISTICS

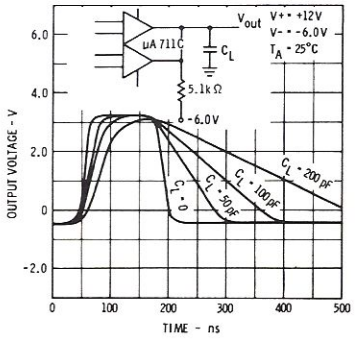
VOLTAGE TRANSFER CHARACTERISTIC



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



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